

Notice of References Cited	Application/Control No. 10/709,362		Applicant(s)/Patent Under Reexamination HATHAWAY ET AL.	
	Examiner Toan M. Le		Art Unit 2863	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-5,508,937	04-1996	Abato et al.	716/6
	B	US-5,944,834	08-1999	Hathaway, David J.	713/500
	C	US-6,772,402	08-2004	Mortensen, Michael Peter	716/6
	D	US-6,789,223	09-2004	Fetherson, R. Scott	714/738
	E	US-6,237,127	05-2001	Craven et al.	716/6
	F	US-6,240,542	05-2001	Kapur, Rajiv	716/12
	G	US-6,553,550	04-2003	Menegay et al.	716/6
	H	US-6,442,741	08-2002	Schultz, Richard T.	716/6
	I	US-6,807,509	10-2004	Bourdin et al.	702/125
	J	US-6,886,152	04-2005	Kong, Raymond	716/16
	K	US-6,799,308	09-2004	You et al.	716/6
	L	US-5,726,902	03-1998	Mahmood et al.	716/6
	M	US-6,536,024	03-2003	Hathaway, David J.	716/6

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Liou et al., False-Path-Aware Statistical Timing Analysis and Efficient Path Selection for Delay Testing and Timing Validation, DAC 2002, Pages 566-569
	V	Chang et al., Statistical Timing Analysis Considering Spatial Correlations Using a Single Pert-Like Traversal, ICCAD 2003, Pages 621-625
	W	Liou et al., Modeling, Testing, and Analysis for Delay Defects and Noise Effects in Deep Submicron Devices, June 2003, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 22, No. 6, Pages 756-769
	X	Agarwal et al., Statistical Delay Computation Considering Spatial Correlations, 2003 IEEE, Pages 271-276

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.